Lab 9: Optimization using Logical Effort

ECEN 454-503

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**Purpose:** This lab serves to introduce the student to the “logical effort and gate sizing” techniques discussed in class. During this lab, I identified the critical path in my previously designed 4-bit adder and reduced its delay by determining the optimal number of devices and ideal sizes of the gates along this path.

**Procedure:**

1. Draw a gate-level schematic of a 4-bit adder and find the critical path.
2. Calculate the number of stages in the circuit, path effort, and transistor sizes.
3. Generate waveforms for the same input vectors as in Lab 5.
4. Make a table comparing delays and VDD Power Consumption of both non-optimized and optimized circuits for all input vectors from step 3.
5. Make a table comparing the Area (sum of all transistors’ W\*L).

**Results:**

1. The gate-level schematic of the 4-bit adder is included below. The critical path is indicated in red in Figure 2, and it can be seen that it contains 1 XOR gate and 8 NAND gates.

*Figure 1: 4-bit Adder Transistor-level Schematic*

*A screen shot of a computer

Description automatically generated with low confidence*

*Figure 2: 4-bit Gate-level Schematic & Critical Path*

*A picture containing diagram

Description automatically generated*

1. The required calculations for this lab were performed as follows:
   1. Cnand = 1.9967 fF
   2. Cxor = 6.3029 fF
   3. Cload = 30 fF
   4. H = Cload / Cxor = 4.7597
   5. wp, non-optimized = 600 nm
   6. wn, non-optimized = 300 nm
   7. l non-optimized = l optimized = 200 nm
   8. Gxor, non-optimized = Gxor, optimized = (2\*wp+2\*wn)/(wp/2+wn/2) = 4
   9. Gnand, non-optimized = (wp+wn)/(wp+wn/2) = 1.2
   10. Gnon-optimized = Gxor, non-optimized \* (Gnand, non-optimized)^8 = (1024\*( wp+wn) 8 )/( 2\*wp+wn) 8 = 17.1993
   11. b1 = (Cxor+Cnand)/Cxor = 1.3168
   12. b2 = b4 = b6 = b8 = (Cnand+Cxor)/Cnand = 4.1567
   13. b3 = b5 = b7 = b9 = Cnand/Cnand = 1
   14. B = b1\*b2\*b3\*b4\*b5\*b6\*b7\*b8\*b9 = 393.092
   15. F = G\*B\*H = (1.9159\*(wp+wn) 8/9)/(2\*wp+wn) = 32,179.9
   16. ˆf = F1/9 = 3.1684
   17. Area non-optimized = 4\*(2\*Axor + 3\*Anand) = 72\*(200\*wp+200\*wn) = 14,400\*(wp+wn) = 12.96 µm^2
   18. Cin, 9 = 30 fF
   19. Cin, 8 = (g8\*Cout, 8)/ ˆf = 11.3622, k = 11.3622/1.9967 = 5.69049600 => wp = 3414.29 nm, ˆf = 2.7949
   20. Cin, 7 = (g7\*Cout, 7)/ ˆf = 4.8783, k = 4.8783/1.9967 = 2.4432 => wp = 1465.92nm, ˆf = 2.7949
   21. Cin, 6 = (g6\*Cout, 6)/ ˆf = 2.0945, k = 2.0945/1.9967 = 1.04899 => wp = 629.393, ˆf = 3.15071
   22. Cin, 5 = (g5\*Cout, 5)/ ˆf = 0.797725, does not need to be resized
   23. Cin, 4 = (g4\*Cout, 4)/ ˆf = 0.3004, does not need to be resized
   24. Cin, 3 = (g3\*Cout, 3)/ ˆf = 0.113, does not need to be resized
   25. Cin, 2 = (g2\*Cout, 2)/ ˆf = 0.0426, does not need to be resized
   26. Cin, 1 = (g1\*Cout, 1)/ ˆf = 0.05349, does not need to be resized
2. The next 4 figures show the optimized pre-layout waveforms for the input vectors in Lab 5 after making all the necessary adjustments to the 4-bit adder.

*Figure 3: A=0000 B=1111 Cin=1*

*Graphical user interface

Description automatically generated with low confidence*

*Figure 4: A=1010 B=0101 Cin=0*

*A picture containing graphical user interface

Description automatically generated*

*Figure 5: A=1010 B=0101 Cin=1*

*A picture containing text

Description automatically generated*

*Figure 6: A=1100 B=1000 Cin=0*

*A computer screen capture

Description automatically generated with medium confidence*

1. The tables below include the delays and VDD Power Consumptions for the non-optimized and the optimized circuits (using the same inputs as in the previous part).

*Table 1: Optimized vs. Non-Optimized Delays*

|  |  |  |  |
| --- | --- | --- | --- |
| **Input** | **Output** | **Non-Optimized Time (ns)** | **Optimized Time (ns)** |
| **A: 0000**  **B: 1111**  **Cin: 1** | Cout  S<0>  S<1>  S<2>  S<3> | 1.763  1.101  1.101  1.103  1.103 | 1.5897  1.1667  1.1667  1.1665  1.1663 |
| **A: 1010**  **B: 0101**  **Cin: 0** | Cout  S<0>  S<1>  S<2>  S<3> | 1.7387  1.114  1.101  1.114  1.104 | 1.5877  1.0899  1.0910  1.0899  1.0905 |
| **A: 1010**  **B: 0101**  **Cin: 1** | Cout  S<0>  S<1>  S<2>  S<3> | 1.1762  1.1017  1.1147  1.1017  1.1147 | 1.621  1.0899  1.0546  1.0899  1.0546 |
| **A: 1100**  **B: 1000**  **Cin: 0** | Cout  S<0>  S<1>  S<2>  S<3> | 0.5264  0.7937  1.155  1.105  1.4959 | 0.4952  1.0546  1.0852  1.0758  1.0985 |

*Table 2: VDD Power Consumption (Optimized vs. Non-Optimized)*

|  |  |  |
| --- | --- | --- |
| **Case** | **Non-Optimized Power (µW)** | **Optimized Power (µW)** |
| **A: 0000**  **B: 1111**  **Cin: 1** | -192.8 | -158.5 |
| **A: 1010**  **B: 0101**  **Cin: 0** | -192.7 | -158.3 |
| **A: 1010**  **B: 0101**  **Cin: 1** | -193.2 | -159.1 |
| **A: 1100**  **B: 1000**  **Cin: 0** | -128.1 | -108.5 |

1. Lastly, the following table compares the area of the non-optimized vs. the optimized circuits.

*Table 3: Optimized vs. Non-Optimized Area*

|  |  |  |
| --- | --- | --- |
|  | Non-Optimized | Optimized |
| Area (µ2m2) | 12.96 | 13.702 |

**Conclusion:** This lab helped me better understand how to apply logical effort and gate sizing techniques in order to optimize my 4-bit adder design.